Independent claims 1 and 13 recite a method for manufacturing a trench field effect transistor. As amended, claim 1 recites a method including "after substantially filling the first trench with conductive material, forming a source region having the first conductivity type inside the body region and adjacent to the first trench." Claim 13 recites a method including "after substantially filling the first trench with polysilicon, implanting impurities of the first conductivity type inside the body region to form a source region adjacent to the first trench." In other words, the source region is not formed until after the gate trench has been formed and filled.

In contrast, Takahashi discloses a method in which the source layer 24 is formed by ion implantation *before* the gate trench is formed and filled, as shown in Fig. 4A (see also col. 5, lines 37-39). This ordering of steps cannot be reversed because Takahashi further discloses that the gate oxide film 25, polysilicon layer 26, and interlayer insulator 27 that fill the gate trench also extend over "a trench peripheral surface portion of the source layer 24" (col. 5, lines 7-10; see Figs. 3, 4C). If these layers were formed before the ion implantation step that forms the source layer, the polysilicon would preclude formation of a source region for the transistor. In the method of the present invention, the conductive material that fills the gate trench does not extend over a surface portion of the substrate peripheral to the trench (as shown, e.g., in Fig. 2A), so that it is possible to form the source region *after* filling the gate trench, as recited in claims 1 and 13. The claimed method is simpler than the method of Takahashi, which requires additional masking and etching steps to form spaces between the surface extensions of different gate electrodes and to form side insulator layers 30 over the ends of the surface extensions (col. 5, lines 40-55; see Figs. 4B-4E). The methods recited in claims 1 and 13 do not require such steps. Thus, Takahashi does not disclose or suggest the sequence of steps recited in claims 1 or 13, in which the source region is formed *after* filling the gate trench.

For at least this reason, Applicants respectfully submit that claims 1 and 13 are patentable over Takahashi. Further, because claims 2, 3, 6-8, and 12 depend from

claim 1, and claims 14 and 15 depend from claim 13, these claims are also patentable for at least this reason. Withdrawal of the rejection under §102(e) is respectfully requested

New Claims 18-21

Claims 18-21 have been added by this amendment. Applicants respectfully submit that these claims are supported by the specification, e.g., in Fig. 2B.

In order to expedite prosecution, Applicants respectfully submit herein grounds for patentability of new claims 18-21 over Takahashi. First, claims 18-19 and 20-21 depend from claims 1 and 13, respectively, and are therefore patentable over Takahashi for at least the reasons stated above. Second, claims 18-21 each recite further features of the present invention that are not taught or suggested by Takahashi.

Claims 18 and 20 each recite that the first trench (i.e., the gate trench) is substantially completely filled with conductive material (claim 18) or polysilicon (claim 20), which is not taught or suggested by Takahashi. Instead, Takahashi teaches that the gate trench is only partially filled with a polysilicon layer 26 and that the rest of the trench is filled with an interlayer *insulator* film 27 (Figs. 3 and 4B; col. 5, lines 9-12). There could be found in Takahashi no suggestion that interlayer insulator 27 can be omitted or that the gate trench can be completely filled with conductive material. It is noted that filling the gate trench substantially completely with conductive material, as recited in claims 18 and 20, simplifies the manufacturing process by eliminating at least the step of depositing interlayer insulator film 27. Claims 18 and 20 are patentable over Takahashi for at least this reason also.

Claims 19 and 21 each recite that the conductive material (claim 19) or polysilicon (claim 21) that fills the gate trench "does not extend over a substantial portion of the substrate surface peripheral to the first trench." In contrast, Takahashi teaches that conductive layer 27 does extend over "a trench peripheral surface portion of the source layer 24" (col. 5, lines 7-10; see Figs. 3, 4C). As discussed above, not extending these materials over the surface of the substrate, as recited in claims 19 and 21, considerably

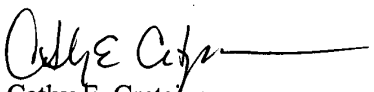
simplifies the manufacturing process. Claims 19 and 21 are patentable over Takahashi for at least this reason also.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A method of manufacturing a trench field effect transistor on a substrate having a first conductivity type, the method comprising the steps of:

forming a first trench extending into the substrate;

lining the first trench with dielectric material;

substantially filling the first trench with conductive material to form a gate electrode of the field effect transistor;

forming a body region having a second conductivity type in the substrate;

after substantially filling the first trench with conductive material, forming a source region having the first conductivity type inside the body region and adjacent to the first trench;

forming a second trench adjacent to said source region, the second trench defined by sidewalls extending into the body region and a bottom, which terminates below the source region and in contact with the body region; and

filling the second trench with high conductivity material for making contact to the body region.

2. The method of claim 1 wherein the step of filling the second trench with high conductivity material for making contact to the body region also makes contact to the source region.

3. The method of claim 2 wherein the step of filling the second trench with high conductivity material comprises a self-aligned masking step for making contact with both the body region and the source region.

6. The method of claim 2 further comprising a step of forming a thin layer of barrier metal between the high conductivity material and the body region.

7. The method of claim 6 wherein the high conductivity material comprises aluminum and the thin layer of barrier metal comprises titanium.

8. The method of claim 2 wherein the step of forming the second trench comprises a step of etching silicon through the source and body regions.

12. The method of claim 8 wherein the step of etching etches the silicon at an angle resulting in a slanted edge along the etched side of the source region.

13. (Twice Amended) A process for manufacturing a trench field effect transistor comprising the steps of:

etching a first trench in a substrate having a first conductivity type;

lining the first trench with a layer of dielectric material;

substantially filling the first trench with polysilicon;

implanting impurities of a second conductivity type into the substrate to form a body region having the second conductivity type over the substrate;

after substantially filling the first trench with polysilicon, implanting impurities of the first conductivity type inside the body region to form a source region adjacent to the first trench;

etching a second trench through the source region and into the body region, the second trench defined by sidewalls and a bottom, which terminates in contact with the body region; and

filling the second trench with metal making contact with both the source region and the body region.

14. The process of claim 13 further comprising a step of implanting impurities of the second conductivity type into the body region under the second trench before the step of filling the second trench with metal.

15. The process of claim 13 wherein the step of etching the second trench etches the second trench to a shallower depth than the first trench.